PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference FIS920020139	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US02/41181	International filing date *(day/month/year)* 20 December 2002 (20.12.2002)	Priority date *(day/month/year)*
International Patent Classification (IPC) or national classification and IPC IPC(7): H01L 21/44, 21/48, 21/50, 21/331, 21/30, 21/46 and US Cl.: 438/109, 118, 367, 459, 612, 977		
Applicant INTERNATIONAL BUSINESS MACHINES CORP.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
20 July 2004 (20.07.2004)	15 October 2004 (15.10.2004)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer David E Graybill DEBORAH A. THOMAS PARALEGAL SPECIALIST GROUP 1300 Telephone No. (571)272-2815

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/41181

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed.

☒ the description:
pages 1-12 as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

☒ the claims:
pages 13 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages 14-16 , filed with the letter of 15 October 2004 (15.10.2004)

☒ the drawings:
pages 1-22 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages none

☒ the claims, Nos. none

☒ the drawings, sheets/~~fig~~ none

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/41181

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1-14	YES
	Claims NONE	NO
Inventive Step (IS)	Claims 1-14	YES
	Claims NONE	NO
Industrial Applicability (IA)	Claims 1-14	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS

Claims 1-14 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the claimed invention as a whole including the steps of bonding the second wafer to the first wafer using the layer of bonding material, so that the stud makes electrical contact with the via.

Claims 1-14 meet the criteria set out in PCT Article 33(4), and thus meet industrial applicability because the subject matter claimed can be made or used in industry.

---------- NEW CITATIONS ----------

AMENDED CLAIMS
[received by the International Bureau on 08 July 2003 (08.07.03);
original claims 5, 6, 9 and 11-14 amended]

forming a layer of conducting material (24) in said opening;

providing a third wafer (3) having a front surface (3a), the third wafer having devices formed therein adjacent to the front surface thereof;

forming a stud (37) on the front surface (3a) of the third wafer;

forming a layer of bonding material (36) on the front surface (3a) of the third wafer, the studs projecting vertically therefrom;

aligning the stud (37) to the opening (23) in the back surface of the second wafer; and

bonding the third wafer to the second wafer using the layer of bonding material (36), so that the stud (37) of the third wafer makes electrical contact with the via (22) of the second wafer, with the stud (27) of the second wafer, and with the via (12) of the first wafer.

3. A method according to claim 1 or claim 2, characterized in that said step of removing material causes the wafer to have a thickness of less than 20μm.

4. A method according to claim 1 or claim 2, further comprising the step of attaching a handling plate (15) to the front surface (1a) of the first wafer (1) using a layer of bonding material (16).

5. A method according to claim 1 or claim 2, further comprising the step of forming a conducting body (102) in one of the first wafer (1) and the second wafer (2) and connecting to the via (12/22) in the wafer, the conducting body extending laterally under the devices of the wafer, and characterized in that the opening (103) in the back side of the wafer is separated laterally from the via in accordance with the lateral extent of the conducting body (102).

AMENDED SHEET (ARTICLE 19)

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6. A method according to claim 1 or claim 2, further comprising the steps of:
forming an additional opening (113) in the back surface of the first wafer;
forming an additional layer of conducting material (114) in said additional opening;
forming an additional stud (127) on the front surface of the second wafer; and
aligning the additional stud (127) to the additional opening (113) in the back surface of the first wafer;
and characterized in that said step of bonding the second wafer to the first wafer forms a connection between the additional stud (127) and the additional layer of conducting material (114) for conducting heat between the second wafer and the first wafer.

7. A method according to claim 6, characterized in that the additional layer of conducting material (114) is electrically insulated from the via (12).

8. A method according to claim 2, further comprising the steps of:
forming an additional opening in the back surface of the second wafer;
forming an additional layer of conducting material in said additional opening;
forming an additional stud on the front surface of the third wafer; and
aligning the additional stud to the additional opening in the back surface of the second wafer;
and characterized in that said step of bonding the third wafer to the second wafer forms a connection between the additional stud and the additional layer of conducting material for conducting heat between the third wafer and the second wafer.

9. A method according to claim 1 or claim 2, characterized in that said bonding material is a thermoplastic material.

10. A method according to claim 9, characterized in that the thermoplastic material is polyimide.

AMENDED SHEET (ARTICLE 19)

11. A method according to claim 1 or claim 2, further comprising the step of attaching the three-dimensional integrated device (100) to a multichip module (300).

12. A method according to claim 1 or claim 2, further comprising the step of attaching the three-dimensional integrated device (401) to an insulating layer having wiring formed therein (450) using a stud-via connection.

13. A method according to claim 2, characterized in that the first wafer and second wafer have cache memory devices, and the third wafer has logic devices.

14. A method according to claim 2, characterized in that at least one of the first wafer, the second wafer and the third wafer includes a MEMS device.